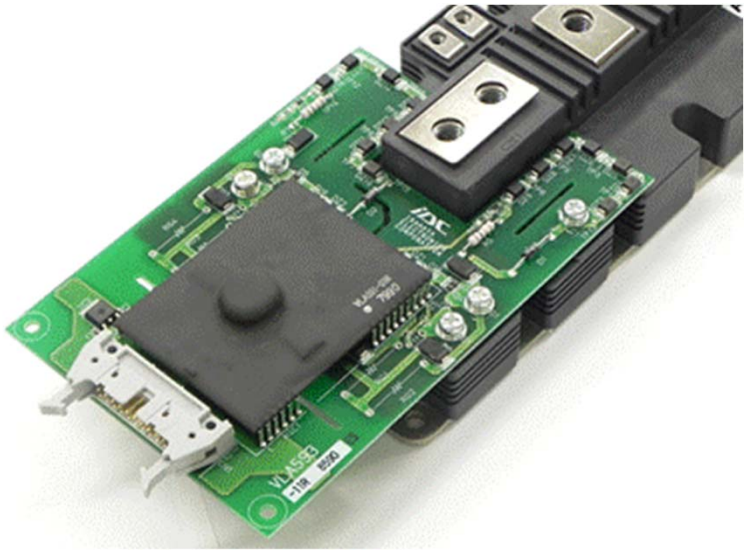
Preliminary

IGBT Gate Drive Unit
VLA593-11R



Sep.2021

IGBT Gate Drive Unit VLA593-11R

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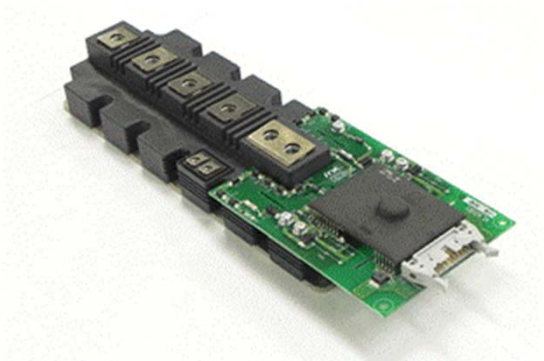
Features

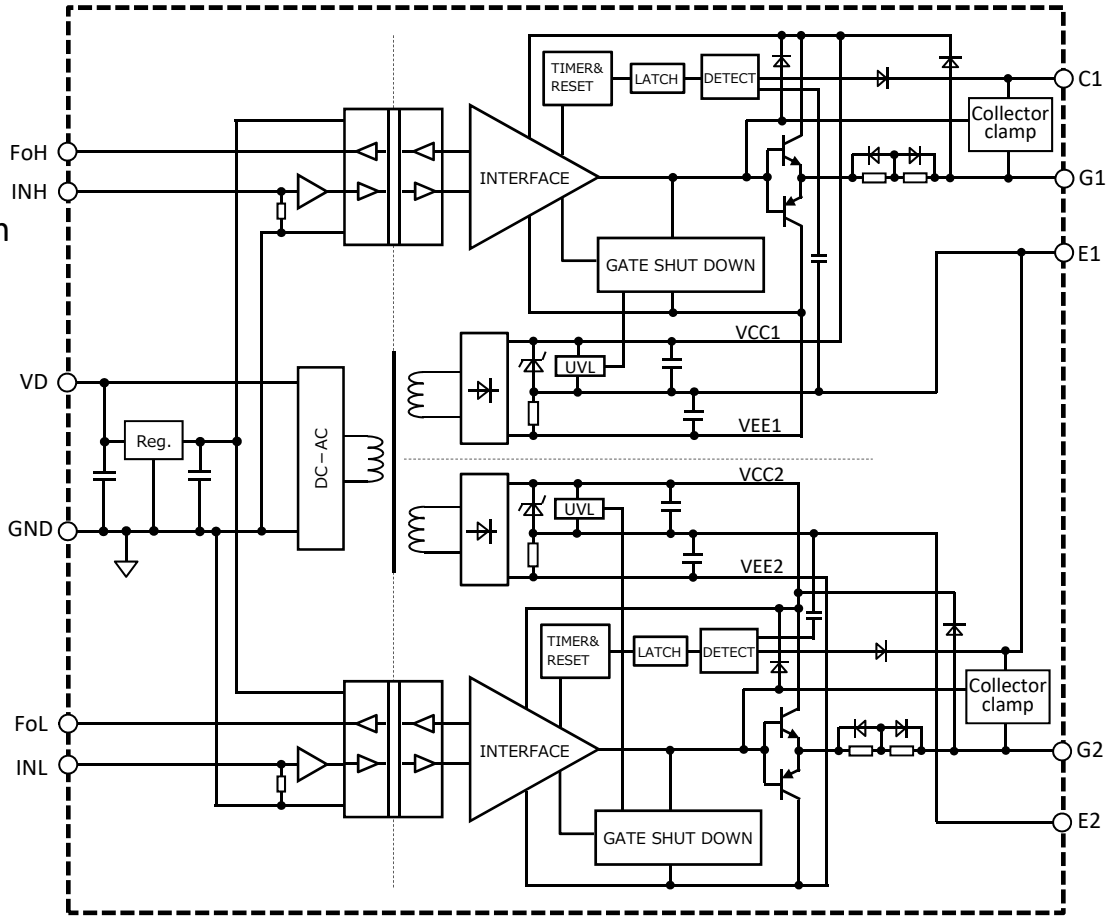
>Directly mountable on the Prime PACK
>Built in the isolated DC-DC converter for gate drive
>Output peak current is +/-20A(max)
>Electrical isolation voltage is 4000Vrms
(for 1 minute)
>Built in short circuit protection with soft shut down
>Built in collector clamp circuit
>One way power supply system for drivers and
input signal (VD=15V)

Targeted IGBT Modules

1700V series Prime PACK IGBT modules



Block Diagram



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Maximum ratings

(unless otherwise noted, Ta=25C)

Symbol	Item	Conditions	Ratings	Unit
VD	Supply voltage	DC	-1 ~ 16.5	V
VI	Input signal voltage	Applied between GND - INH,INL	19	V
I_Fo	Fo output current	Sink and source current of Fo terminal	+/-10	mA
IOHP	Output peak current	Pulse width 3us	-20	A
IOLP			20	A
Viso	Isolation voltage between primary and secondary	Sine wave voltage 60Hz, for 1min	4000	Vrms
Topr	Operating temperature	No condensation allowable	-40 ~ 85	deg C
Tstg	Storage temperature	No condensation allowable	-40 ~ 90	deg C
Idrive	Gate drive current	Gate average current (Per one circuit)	100	mA
VDC_Link	Main circuit voltage	The voltage between P and N	1200	V

Electrical characteristics

(unless otherwise noted, Ta=25 degC, VD=15V, f=3kHz)

Symbol	Item	Conditions	Limits			Unit
			Min	Typ	Max	
VD	Supply voltage	Recommended range	14.5	15	15.5	V
f	Switching frequency	Recommended range It is limited by gate average current (max:100mA)	-	-	7	kHz
RG	Gate resistance	Recommended range	0.5	-	-	ohm
VI	Input signal voltage	Recommended range	4.5	-	15.5	V
I_Fo	Fo output current	Recommended range	-4	-	4	mA
VI_H	Input signal high threshold	-	1.5	1.8	2.1	V
VI_L	Input signal low threshold	-	0.8	1.1	1.4	V
VOH	Plus bias output voltage	Input “H”(High active)	13.5	15.2	16.5	V
VOL	Minus bias output voltage	Input “L”	-6	-8	-11	V
tPLH	“L-H” propagation time	RG=1.5Ω, f=3kHz, C_load:0.33uF	-	0.29	-	us
tPHL	“H-L” propagation time	RG=1.5Ω, f=3kHz, C_load:0.33uF	-	0.15	-	us
ttimer	Timer	Between start and cancel of protection (Under input signal is off state)	1	-	2	ms
UVLO+_VCC	Under voltage lock out	VCC voltage (Operation start)	-	12.6	-	V
UVLO-_VCC	Under voltage lock out	VCC voltage (Operation stop)	-	11.7	-	V
Vz (*1)	Clamp zener voltage	Total zener voltage in collector clamp circuit at Iz = 1mA , Tj=25 deg C	1270	1340	1410	V
VSC	SC detect voltage	Collector voltage of IGBT	15	-	-	V

*1 : It depends on the condition of use, but actual clamp voltage of collector approximately rises by 300V from 200V to Vz.

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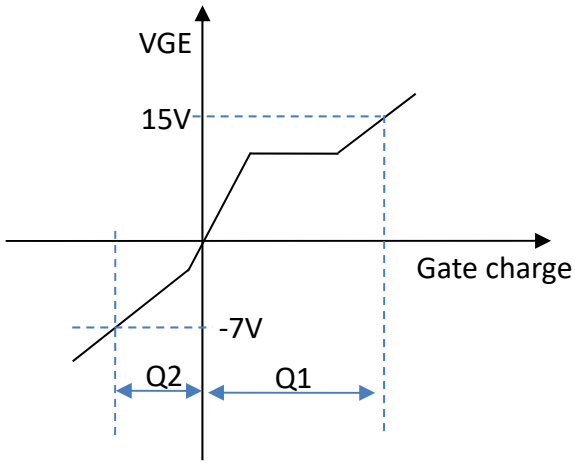
Calculation for gate drive current (gate average current)

This product has isolated DCDC converter built in for gate drive.
The maximum output average current is 100mA per one channel.
This current means maximum gate average current.
When you decide the switching frequency,
please check the gate average current by next formula.

Idrive = (Q1＋|Q2|) X f ← It must be less than 100mA
Idrive : Gate average current
Q1 : Gate charge at +15V (Read from data sheet of IGBT)
Q2 : Gate charge at -7V (Read from data sheet of IGBT)
f : Switching frequency of IGBT

Gate charge characteristic of IGBT



Circuit diagram

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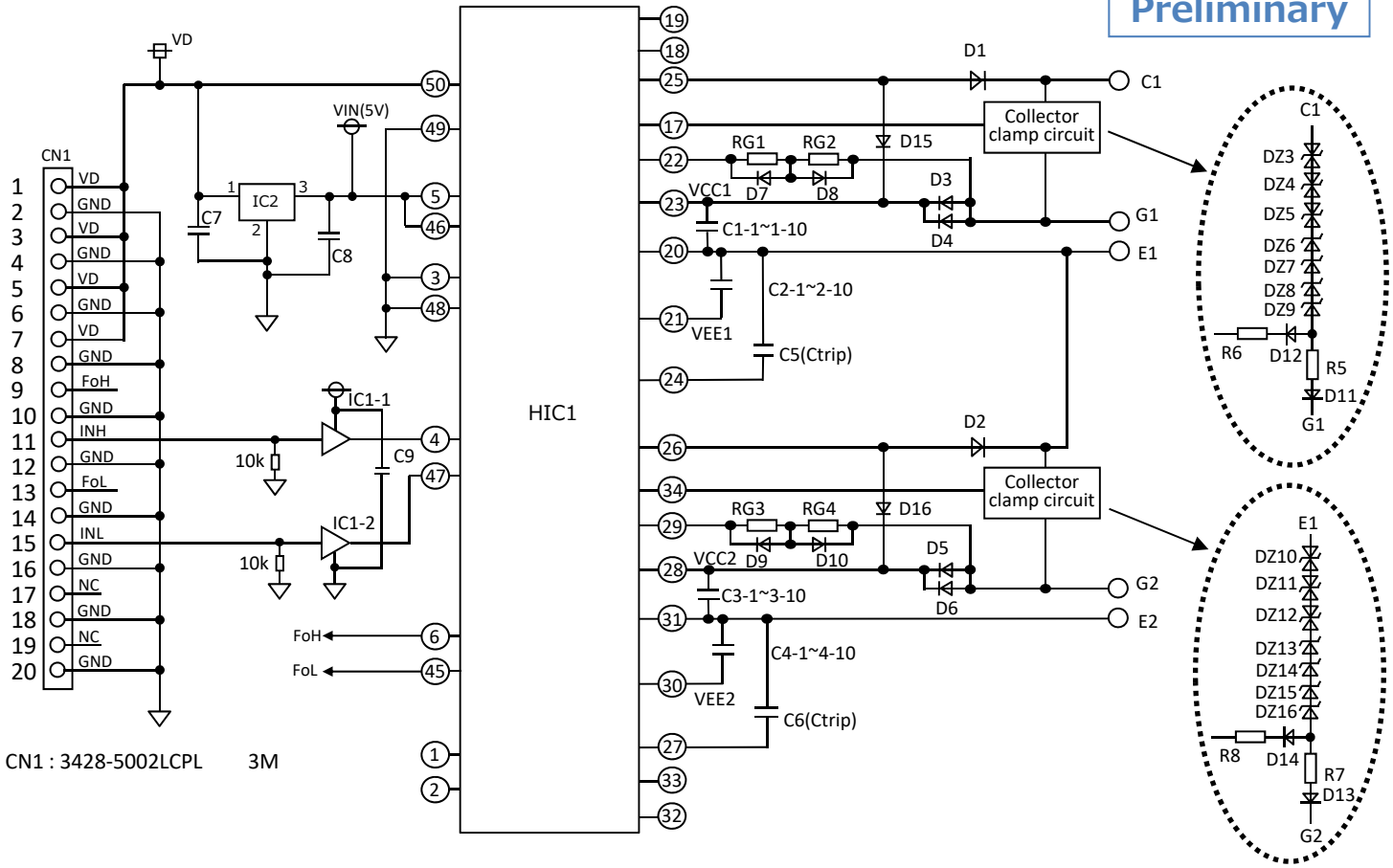
CN1	
Pin N.o.	Pin name
1	VD
2	GND
3	VD
4	GND
5	VD
6	GND
7	VD
8	GND
9	FoH
10	GND
11	INH
12	GND
13	FoL
14	GND
15	INL
16	GND
17	NC
18	GND
19	NC
20	GND



CN1 : 3428-5002LCPL 3M

Note

1)Gate Resistor is not installed at the time of shipment.
Please solder the chosen resistor.

2) C5,6 is not installed at the time of shipment.
It isn't be needed basically.
But if needed, please solder the chosen condenser.
50V, ceramic, ~ 47pF (rough guide)

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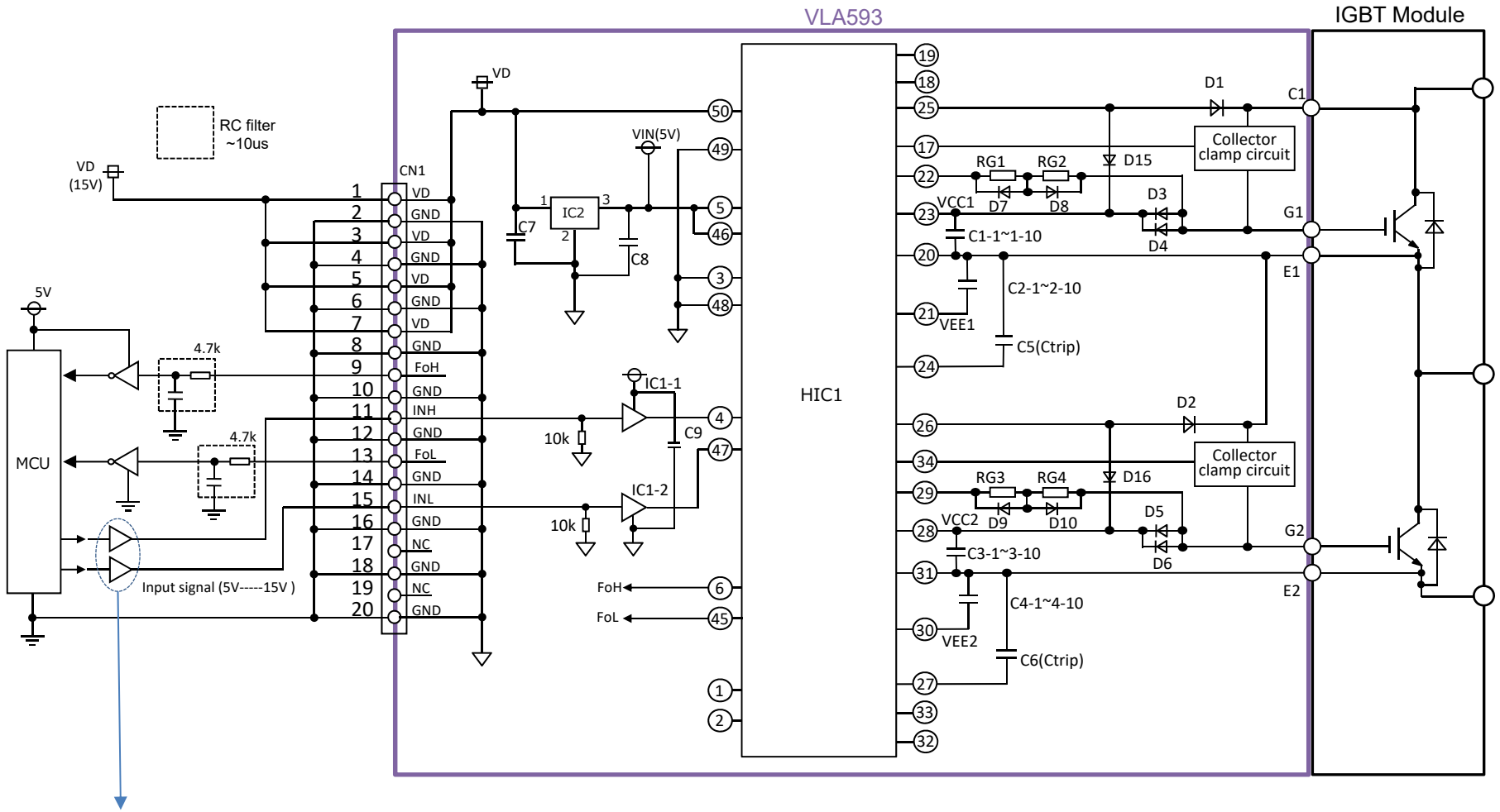
Application example



Note) About the IC which drives gate signal on input side, it is not recommended to use the one whose output is open collector or open drain type.

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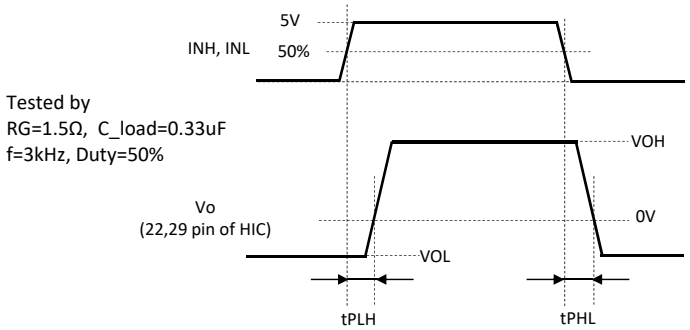
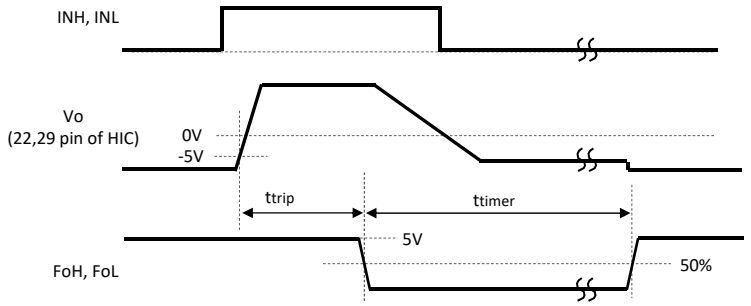
Definition of characteristics

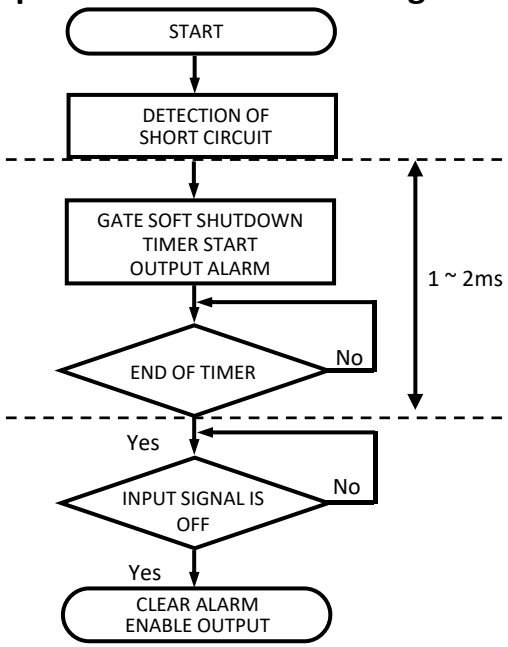
Switching operation



Operation of short circuit protection



Operation flow on detecting short circuit



Operation of protection circuit

(1) In case the gate voltage is “H” and the collector voltage is high, this drive unit will recognize the circuit as short circuit and reduce the gate voltage (soft shut down). Besides, put out error signal (”L”) which inform that protection circuit is operating at the same time from Fo terminal (6,45 pin of CN1).

(2) The protection circuit reset and resort to ordinary condition if input signal is “OFF” when the premised 1~2msec passed. (“OFF” period needs 10us or more)

(3) When the output rises, the masked time detect short circuit (ttrip) is set up so that on-time of IGBT can be secured properly.
It is possible to adjust that time by connecting the capacitor (Ctrip) at the point of C5,6 for countermeasure of misdetection.

Latch & Timer reset system in short-circuit protection circuit

Once the short-circuit protection circuit starts, it shuts down the gate output and keeps alarm output, causing the latch status. This status is canceled if the input signal is OFF when specific time elapses after the activation of the short-circuit protection circuit. Then, gate output depending on input signals becomes possible. If the input signal is ON when specific time elapses, the latch status is not canceled: it is canceled when the signal becomes OFF.

As mentioned above, on the latch & timer reset system, the latch status is resulted after activation of the protection circuit and shutdown of the gate output. Therefore, during this period, gate output is not made no matter how much input signals are received. For this reason, it is possible to safely stop the entire equipment by sending error signals to the microcomputer during this period to stop all gate signals.

Note about collector clamp circuit (1)

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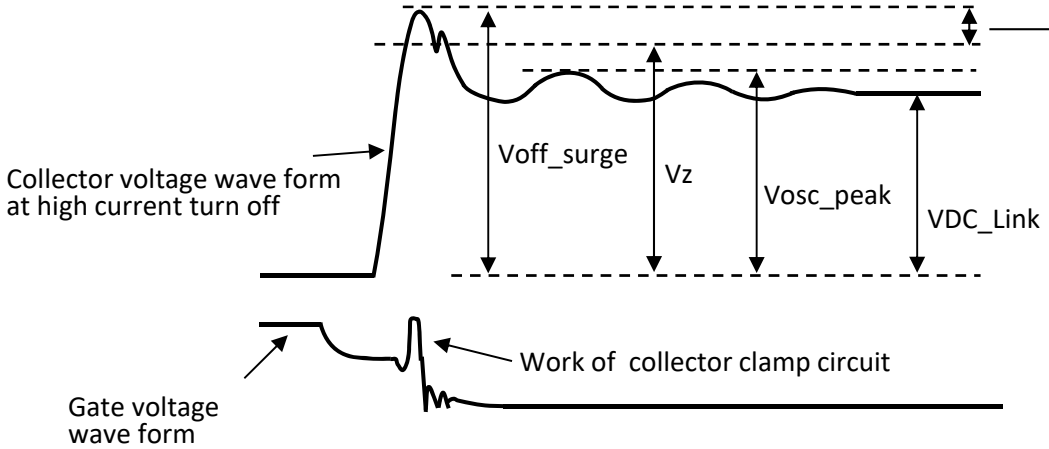
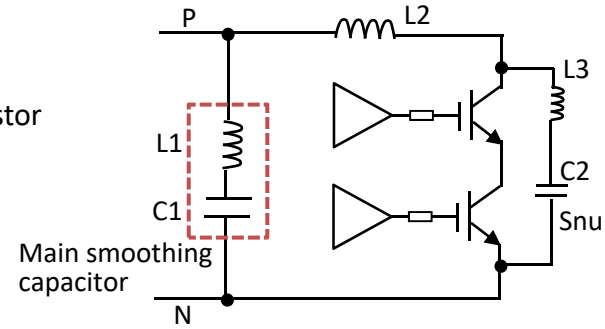
The following chart is the collector voltage wave form of IGBT at high current turn off.
This drive unit has collector clamp circuit built in.
As for this clamp circuit, there is effectiveness to control the surge voltage on collector at high current turn off, but the surge voltage may go over the maximum rating of collector voltage depending on the condition of use.
Therefore please confirm it in the actual machine evaluation.
Finally each parameter must be the following relation. Please keep this condition.

VDC_Link < Vosc_peak < Vz < Voff_surge



The next countermeasures are effective to suppress the rise and oscillation of the collector voltage.

(1) Reducing the value of L1,L2 and L3
(2) Increasing the value of C2
(3) Increasing the resistance of off gate resistor
(4) Limiting maximum collector current
(5) Reducing the VDC_Link



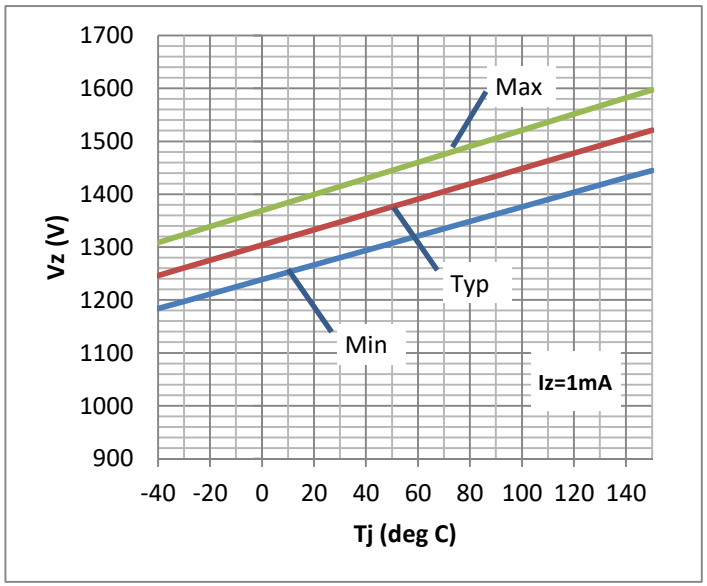
L1:Stray inductance in main smoothing capacitor
L2:Stray inductance of main wiring
L3:Stray inductance of snubber circuit
C1:Main smoothing capacitor
C2:Snubber capacitor

Note about collector clamp circuit (2)

Preliminary

The total zener voltage in the collector clamp circuit has the tolerance and fluctuation by temperature such as the following chart.
Please keep the main circuit so that the DC_Link voltage does not exceed this zener voltage.

Total zener voltage characteristic



Note about collector clamp circuit (3)

When the collector clamp circuit operates repeatedly, it may be destroyed for heat.
Therefore please keep it to work non-consecutively.

About mounting gate resister

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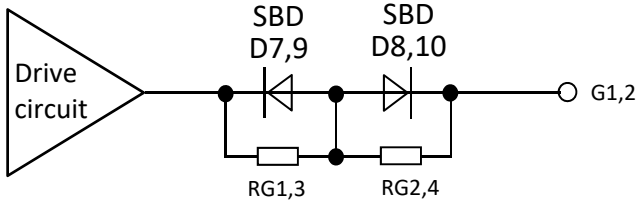
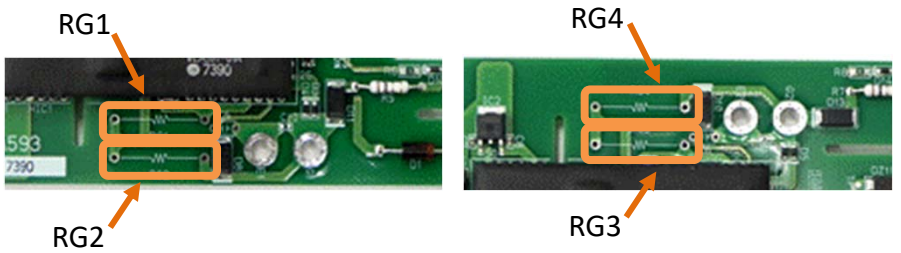
There is not Gate Resistors at the initial state.
It is possible to install up to 2 resistors in mount area of gate resistor per one channel.
And there are some variations by combining resistor.
There are some examples in the following chart, please refer to it and set the gate resistor.
And please solder the chosen resistor.

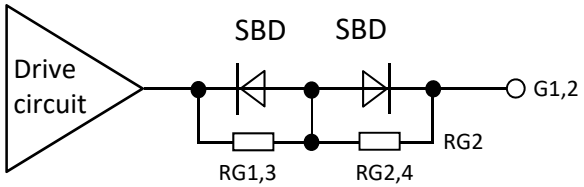




Layout pattern connection on substrate

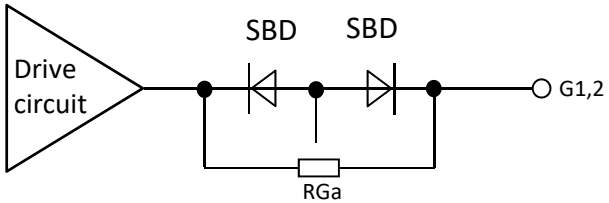
: Gate resistor mount part (Initial is open)

Example 1



RG_on ➔RG1,3
RG_off ➔RG2,4

Example 2



RG_on ➔RGa
RG_off ➔RGa

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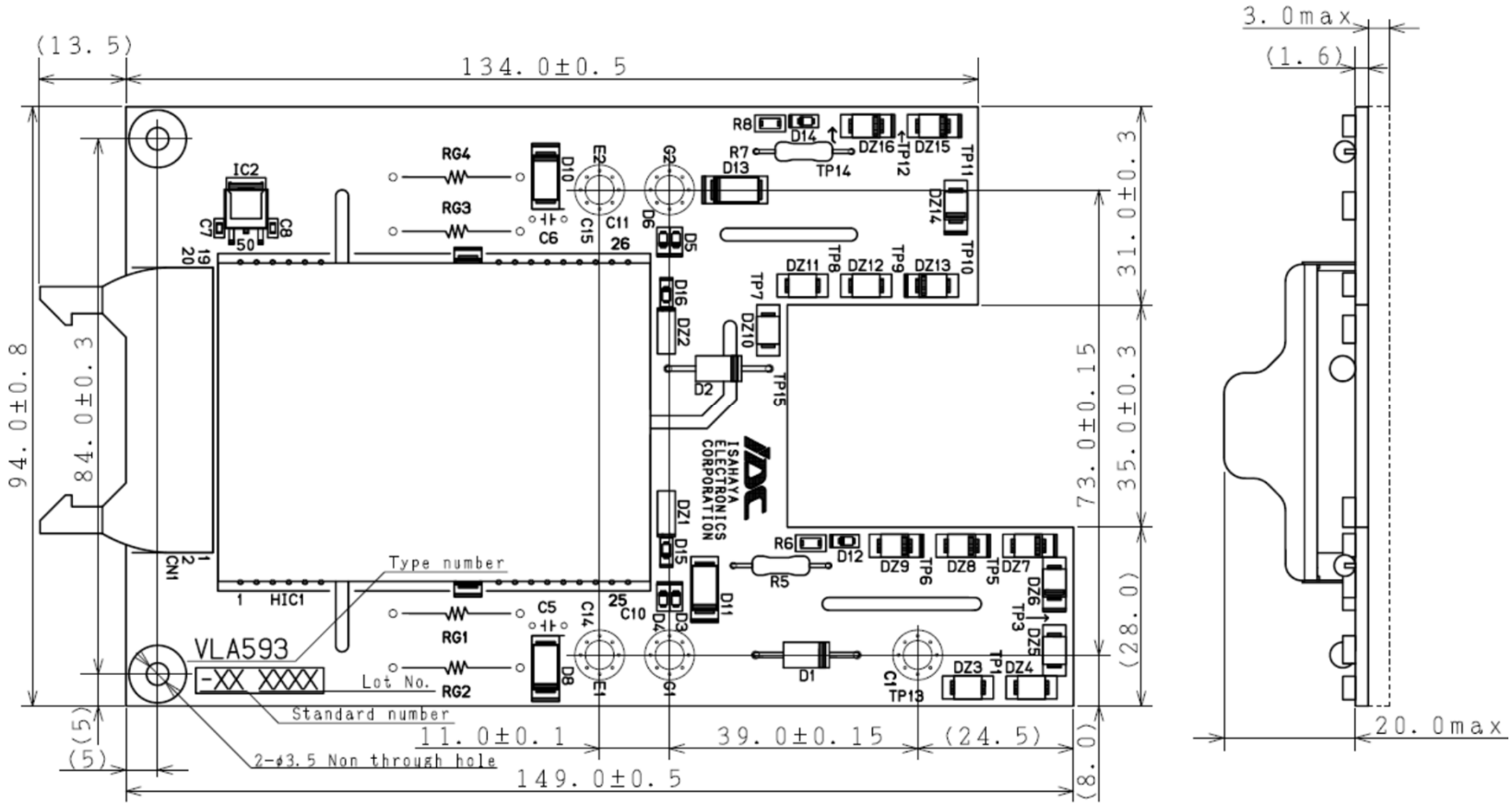
Outline & Size

Note

1) There is not Gate Resistors at the initial state.
   So please solder the chosen resistor.



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